AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A cache memory comprising:

a cache buffer containing most recently accessed data;

a storage array comprising a plurality of cache memory locations and selectively receiving data from said cache buffer, selectively received said data being stored in ones of said memory locations; and

a tag memory storing tags associated with data in said storage array and selected data in said cache buffer, wherein cache power is substantially less for accessing said data in said cache buffer than for accessing data in said storage array.

2. (previously presented) A cache memory as in claim 1, wherein cache input data selectively includes executable commands.

3. (original) A cache memory as in claim 1, wherein said cache buffer comprises:

a cache input buffer receiving cache input data.

4. (previously presented) A cache memory as in claim 3, wherein said cache buffer further comprises:

an output buffer, ones of said tags in said tag memory associated with said most recently accessed data in said output buffer.

5. (original) A cache memory as in claim 4, wherein said tag memory comprises:

a first content addressable memory (CAM) containing tags associated with data stored in said storage array; and

a second CAM containing tags associated with said most recently accessed data.

6. (original) A cache memory as in claim 5, wherein a tag for requested data is checked against tags in said second CAM and said cache input buffer before checking tags in said first CAM.

7. (original) A cache memory as in claim 5, wherein each of said first CAM and said second CAM are a circulating first in first out register (FIFO).

8. (original) A cache memory as in claim 4, wherein each said storage array is a static random access (SRAM) array.

9. (canceled).

10. (previously presented) A content addressable memory (CAM) random access memory (RAM) cache comprising a plurality of CAMRAM banks, each of said CAMRAM banks comprising:

a cache buffer containing most recently accessed data and receiving cache input data, said cache input data selectively including executable commands, wherein said cache buffer comprises:

an input buffer line receiving a cache input data line, and

an output buffer containing said most recently accessed data, ones of said tags in said CAM being associated with said most recently accessed data;

a bank store comprising a plurality of cache memory locations and selectively receiving data from said cache buffer, selectively received said data being stored in ones of said memory locations; and

a CAM storing tags associated with data in said storage array and selected data in said cache buffer, wherein said CAM comprises:

an n-CAM having n tag locations, each n-CAM tag location being associated with one of n storage locations in said bank store, and

an i-CAM containing i tag locations, wherein n > i and each i-CAM tag location is associated with a location in said output buffer, wherein each of said n-CAM and said i-CAM are a circulating first in first out register (FIFO).

11. (canceled)

12. (currently amended) A CAMRAM as in claim 10 [[11]], further comprising a cache storage buffer, each said input buffer line in said plurality of CAMRAM banks being a line in said cache storage buffer.

13. (canceled)

14. (currently amended) A CAMRAM as in claim 10 [[13]], further comprising means for checking a tag for requested data against tags in said i CAM and said cache input buffer independent of tags in said n CAM.

15. (original) A CAMRAM as in claim 14, wherein said checking means only checks for said tag in said n CAM, when said tag is not found in said i CAM or in said cache input buffer.

16. (original) A CAMRAM as in claim 15, wherein cache power is substantially less for accessing said data in said cache buffer than for accessing data in said bank store.

17. (canceled)

18. (original) A CAMRAM as in claim 11, wherein said bank store is a static random access (SRAM) array.

19. (currently amended) A method of managing data in a cache, said method comprising the steps of:

a) providing incoming data to an input buffer;

b) selectively loading data from said input buffer into a storage array;

c) selectively loading accessed data from said storage array to an output buffer, a number of most recently accessed data blocks being held in said output buffer; [[and]]

d) selectively providing data from each of said input buffer, said storage array and said output buffer responsive to an access request;

e) receiving an access request for data;

f) checking said input data buffer for data requested for access; and

g) checking said output buffer for said data requested for access, wherein said output buffer is checked in step (g) coincident with checking said input buffer in step (f).

20 – 22 (canceled)

23. (currently amended) A method of managing data as in claim 19 [[22]], wherein said access request is a store request and said method further comprises the steps of:

h) storing said data in said output buffer; and

i) marking said stored data as dirty.

24. (canceled)

25. (currently amended) A method of managing data as in claim 19 [[22]], wherein whenever said data requested for access is not found in said output buffer or said input buffer, said method further comprises the steps of:

h) checking said storage array for said data requested for access.

26. (previously presented) A method of managing data as in claim 25, wherein whenever said data requested for access is found in said storage array, said method further comprises the steps of:

i) loading said data requested for access into said output buffer; and
j) providing said data requested for access as an output.

27. (previously presented) A method of managing data as in claim 25, wherein whenever said data requested for access is not found in said storage array, said method further comprises the steps of:

i) sending a miss request;
j) loading said input buffer; and
k) providing said data from said input buffer as an output.

28. (previously presented) A method of managing data as in claim 27, wherein whenever said input buffer contains data other than said data requested for access, said sending step (h) further comprises loading other said data from input buffer to said output buffer.

29. (previously presented) A method of managing data as in claim 25, wherein data in each of said input buffer, said storage array and said output buffer are identified by tags, said tags being checked in checking steps (f), (g) and (h).

30. (new) A cache memory comprising:

a cache buffer containing most recently accessed data, wherein said cache buffer further comprises an output buffer, ones of said tags in said tag memory associated with said most recently accessed data in said output buffer;

a storage array comprising a plurality of cache memory locations and selectively receiving data from said cache buffer, selectively received said data being stored in ones of said memory locations; and

a tag memory storing tags associated with data in said storage array and selected data in said cache buffer, wherein said tag memory comprises:

a first content addressable memory (CAM) containing tags associated with data stored in said storage array, and

a second CAM containing tags associated with said most recently accessed data, wherein each of said first CAM and said second CAM are a circulating first in first out register (FIFO).

31. (new) A content addressable memory (CAM) random access memory (RAM) cache comprising a plurality of CAMRAM banks, each of said CAMRAM banks comprising:
a cache buffer containing most recently accessed data and receiving cache input data, said cache input data selectively including executable commands, wherein said cache buffer comprises:

an input buffer line receiving a cache input data line, and

an output buffer containing said most recently accessed data, ones of said tags in said CAM being associated with said most recently accessed data;

a bank store comprising a plurality of cache memory locations and selectively receiving data from said cache buffer, selectively received said data being stored in ones of said memory locations; and

a CAM storing tags associated with data in said storage array and selected data in said cache buffer, wherein said CAM comprises:

an n-CAM having n tag locations, each n-CAM tag location being associated with one of n storage locations in said bank store,

an i-CAM containing i tag locations, wherein n > i and each i-CAM tag location is associated with a location in said output buffer; and

means for checking a tag for requested data against tags in said i CAM and said cache input buffer independent of tags in said n CAM, wherein said checking means only checks for said tag in said n CAM, when said tag is not found in said i CAM or in said cache input buffer and wherein cache power is substantially less for accessing said data in said cache buffer than for accessing data in said bank store.